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EXAMINER	
JUNG, MICHAEL	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,927	ABERIN ET AL.	
	Examiner	Art Unit	
	MICHAEL JUNG	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17,19-25,27-34 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17,19-25,27-34 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20100503*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In response to a previous Office action mailed on 02/02/2010, the Applicant amended the independent claims 17, 22, 24, 30 and 33 in a reply filed on 05/03/2010 (hereinafter "Reply"). The amendment changed the scope of the independent claims 17, 22, 24, 30 and 33, and, consequently, the scope of their respective dependent claims.

Currently, claims 17, 19-25, 27-34 and 36 are pending.

Response to Arguments

1. Applicant's arguments filed in the Reply with respect to claims 17, 19-23, 30-34, and 36 have been fully considered but they are not persuasive.

Although the Applicant amended the independent claims 17, 22, 30 and 33, the Applicant has failed to overcome the cited references in the previous 35 U.S.C. 103(a) rejections of claims 17, 19-23, 30-34 and 36.

In the Reply, the Applicant argues that neither Takeda nor Takamichi, either alone of in combination, teaches or suggest (1) forming non-plated vent holes both in areas outside of a semiconductor chip mounting area and within the semiconductor chip mounting area (p. 8 of the Reply) and (2) non-plated vent holes that are disposed in both an area of the substrate directly underneath the semiconductor chip and in areas adjacent to but not directly underneath the semiconductor chip (p. 8 of the Reply). The examiner respectfully disagrees.

The Annotated Fig. 11 of Takeda (p. 6 of this Office action) shows the non-plated vent holes 7 that are formed in areas B, B' outside of the semiconductor chip mounting area A and within the semiconductor chip mounting area A (see also rejection of claim

17 below.). The Annotated Fig. 11 of Takeda also shows the non-plated vent holes 7 that are disposed in both an area A of the substrate 1 directly underneath the semiconductor chip 2 and in areas B, B' adjacent but not directly underneath the semiconductor chip 2 (see also rejection of claim 22 below).

2. Applicant's arguments with respect to claims 24, 25 and 27-29 have been considered but are moot in view of the new ground(s) of rejection.

Priority

3. Receipt is acknowledged of papers submitted on 05/24/2010 under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The applicant submitted an information disclosure statement (IDS) on 05/03/2010 after the Office action mailed on 02/02/2010. Since the applicant has met the provisions of 37 CFR 1.97, The IDS is in compliance. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

5. Claims 17, 19-25, 27-34 and 36 are objected to because of the following informalities:

In claim 17, "the vent holes" lack antecedent basis. Please consider amending "vent holes" to --the plurality of vent holes--.

In each of the claims 19, 20, 25 and 34 "the vent holes" lacks antecedent basis.

In each of the claims 27, 28 and 34, "the plurality of vent holes" lacks antecedent basis.

For the claims above, please consider amending "the vent holes" and "the plurality of vent holes" to --the plurality of non-plated vent holes--.

In claim 22, "the chip areas and upper contact areas" lack antecedent basis. Please consider amending "the chip areas and upper contact areas" to --the plurality of chip contacts and the plurality of contact area--.

In each of the claims 24 and 30, "the contact areas" lacks antecedent basis. Please consider amending "the contact areas" to "external contact areas".

In each of the claims 31 and 32, "the chip" lacks antecedent basis. Please consider amending "the chip" to --the semiconductor chip--.

In claim 33, "the upper conducting traces and bottom conducting traces" lacks antecedent basis. Please consider amending "the upper conducting traces and bottom conducting traces" to --the plurality of upper conducting traces and the plurality of bottom conductive traces--.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 24-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 24 contains a new matter recitation of "a plurality of non-plated vent holes through the sheet" that is "in areas of the substrate adjacent to but not outside of the semiconductor chip mounting area". The new matter recitation was not described in the originally-filed disclosure of the instant application. Therefore, at the time the application was field, the Applicant did not have possession of the claimed invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

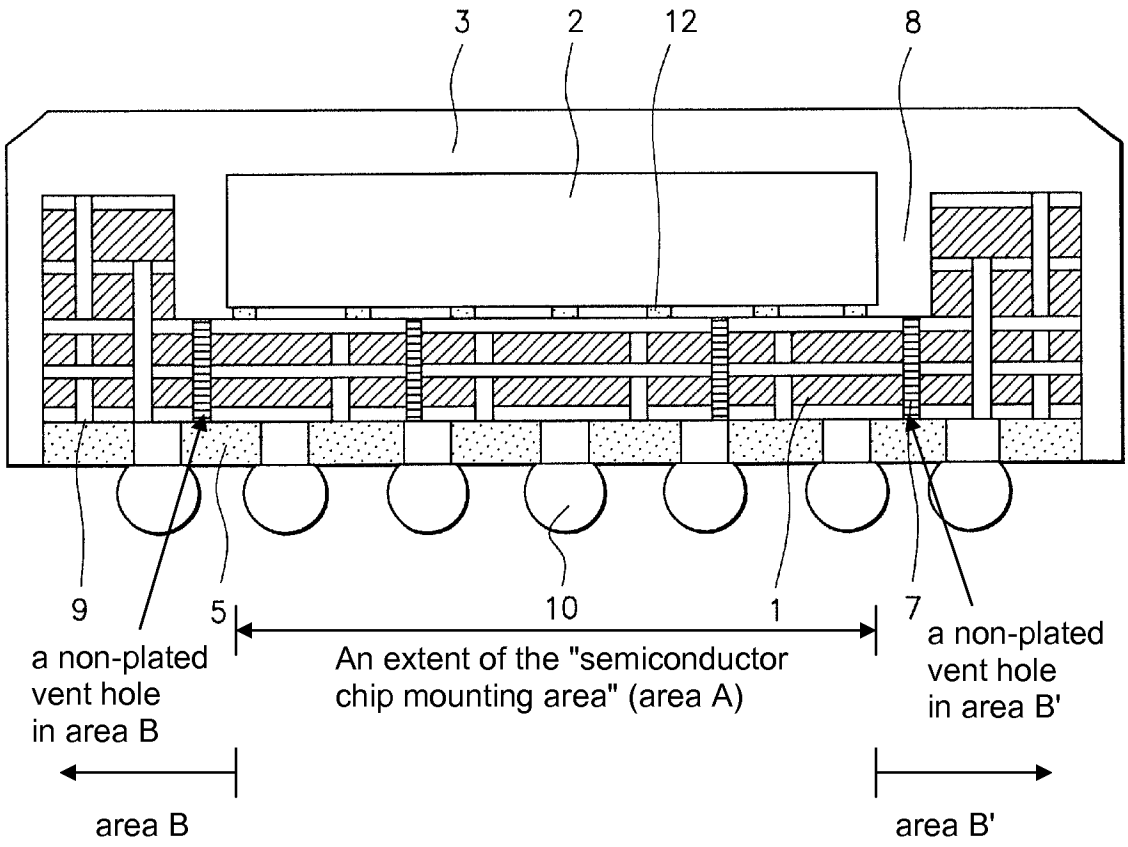
Claim 28 is indefinite for two reasons. First, "the outer edges" lacks antecedent basis. It is unclear which of the edges of the substrate "the outer edges" is referring to. Second, it is unclear what is meant by the plurality of vent holes that are laterally located towards the outer edges of the substrate in view of claim 24, which recites that the plurality of non-plated vent holes are in areas of the substrate adjacent to but not outside the semiconductor chip mounting area. For the purposes of advancing the examination of claim 28, "the plurality of vent holes are laterally located towards...the outer edges of the substrate" has been interpreted to mean that the plurality of vent holes extend towards the outermost edges of the substrate.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 17, 19, 24-34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over unpatentable over Patent No. US 6,014,318 A to Takeda (hereinafter "Takeda") in view of Patent No. US 6,054,755 A to Takamichi et al. (hereinafter "Takamichi").

Annotated Fig. 11 of Takeda



Regarding claim 17, Takeda teaches a method comprising:

providing a substrate 1 (col. 6, ln 23-36 - "Fig. 11 is a sectional side view of a second example of the embodiment of the present invention. At FIG. 11, the wiring substrate 1 is like the same as the first example of the embodiment of the present invention...") comprising a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material") and a plurality of upper conducting traces (Fig. 11 shows the "upper conducting traces" as sections of a third wiring material layer (middle layer) of the five wiring material layers of the substrate 1.) and upper contact pads 12 (col. 6, ln 24-36 - "a bump 12...is formed and the wiring substrate is connected to electrodes (Fig. 11 shows a surface of the third wiring material layer (middle layer).) on an upper surface of the substrate 1, a second plurality of lower conductive traces 11 (col. 6, ln 61-62 - "signal wiring 11 with a conductive material"; Fig. 6 shows a bottommost material layer having a reference character 11. The bottommost material layer having the reference character 11 corresponds to a bottommost wiring material layer of the substrate 1 in Fig. 11.) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on a bottom surface of the substrate and conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and lower conducing traces 11 (see Fig. 11);

forming a plurality of non-plated vent holes through the substrate 1 within a semiconductor chip mounting area A (see Annotated Fig. 11 of Takeda) defined on the upper surface and in areas B, B' (see Annotated Fig. 11 of Takeda) of the substrate 1 adjacent to but outside of the semiconductor chip mounting area A (Annotated Fig. 11 of

Takeda shows two non-plated vent holes 7, 7 within the area A and two non-plated vent holes 7, 7 in the areas B, B'.);

covering the lower surface of the substrate 1 with a layer of solder resist 5 (col. 5, ln 53-55), but leaving the contact areas 10 free from solder resist 5 (see Fig. 11).

Takeda does not disclose a method of covering the upper surface of the substrate with a layer of solder resist.

However, Takamichi teaches a method of covering an upper surface of a substrate 21 (col. 4, ln 8-10) with a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Takeda with the method of covering the upper surface of the substrate with the layer of solder resist as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

As a consequence of the modification, the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the vent holes at the upper surface.

Regarding claim 19, Takeda further teaches the vent holes 7 that include solder resist 5 (col. 6, ln 4-11 - "The inside of this vapor hole is filled with...the same material of solder resist...").

Regarding claim 24, Takeda teaches a substrate 1 (col. 6, ln 4-11) for a semiconductor package (see Fig. 11) comprising:

a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material");

a plurality of upper conducting traces (Fig. 11 shows the "upper conducting traces" as sections of a third wiring material layer (middle layer) of five wiring material layers. "At Fig. 11, the wiring substrate is like the same as the first example of the embodiment of the present invention, the wiring substrate 1 is a multi-layer wiring substrate..." (col. 6, ln 24-36")) and upper contact pads 12 (col. 6, ln 24-36) on an upper surface of the sheet (Fig. 11 shows a surface of the third wiring material layer (middle layer).), a second plurality of lower conductive traces (Fig. 11 shows "lower conductive traces" as sections of the bottommost wiring material layer. Fig. 6 shows a bottommost wiring layer having a reference character 11.) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on a bottom surface of the sheet and a plurality of conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and lower conducing traces 11 (see Fig. 11);

a plurality of non-plated vent holes 7 (col. 6, ln 4-7 - "vapor holes 7") through the sheet within the semiconductor chip mounting area A (Annotated Fig. 11 of Takeda shows two vapor holes 7, 7 situated directly underneath the chip 2.) and in the areas B, B' of the substrate 1 adjacent to the semiconductor chip mounting area A (Annotated Fig. 11 shows a vapor hole 7 formed in an area B to the left of the mounting area and another vapor hole 7 formed in an area B' to the right of the mounting area.); and

a layer of solder resist 5 (col. 5, ln 53-55) covering the lower surfaces of the substrate 1 (see Fig. 11), but leaving the contact areas 10 free from solder resist 5.

Takeda neither discloses a layer of solder resist covering the upper surface of the substrate nor a plurality of non-plated holes that are in areas of the substrate adjacent but not outside of the semiconductor chip mounting area.

However, Takamichi teaches a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C) covering an upper surface of a substrate 21 (col. 4, ln 8-10). Moreover, Takamichi teaches a plurality of non-plated vent holes 24 (col. 4, ln 8-10; see Fig. 1) situated in areas of the substrate adjacent to but not outside of a semiconductor chip mounting area (Fig. 1 shows the non-plated vent holes 24 that are confined within an area defined by the semiconductor chip 26.).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate of Takeda with the layer of solder resist covering the upper surface of the substrate as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate of Takeda by limiting the plurality of vent holes in areas of the substrate adjacent but not outside of the semiconductor chip as taught by Takamichi, with a reasonable expectation of providing sufficient gas permeability (col. 2, ln 43-46).

As a consequence of the modification, the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the plurality of non-plated vent holes at the upper surface.

Regarding claim 25, Takeda further teaches the vent holes 7 that include solder resist (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist...").

Regarding claim 27, the modified substrate as taught by the combination of Takeda and Takamichi teaches the plurality of vent holes that are laterally located towards the center of the substrate (Fig. 11 shows two vapor holes situated directly underneath the center of the semiconductor chip 2.).

Regarding claim 28, the modified substrate as taught by the combination of Takeda and Takamichi teaches the plurality of vent holes that are laterally located towards the center and towards the outer edges of the substrate (Fig. 11 of Takeda has been modified such that the outer vent holes 7, 7 are omitted in light of Takamichi's teaching).

Regarding claim 29, Takeda does not specifically disclose a diameter of the vent hole.

However, Takamichi teaches the vent holes each having a diameter ranging between 0.15 and 0.5 mm (col. 4, ln 23-24).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the diameter of the vent holes of Takeda to range between 0.15 and 0.5 mm as taught by Takamichi, so as to allow moisture produced during the reflow

heating to escape the semiconductor package through the vent holes to prevent delamination (Takamichi, col. 5, ln 14-22).

Regarding claim 30, Takeda teaches a semiconductor package (see Fig. 11) comprising:

a sheet 1 of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material");

a plurality of upper conducting traces (Fig. 11 shows the "upper conducting traces" as sections of a third wiring material layer (middle layer) of five wiring material layers. "At Fig. 11, the wiring substrate is like the same as the first example of the embodiment of the present invention, the wiring substrate 1 is a multi-layer wiring substrate..." (col. 6, ln 24-36")) and upper contact pads 12 (col. 6, ln 24-36) on an upper surface of the sheet (Fig. 11 shows a surface of the third wiring material layer (middle layer).), a second plurality of lower conductive traces (Fig. 11 shows "lower conductive traces" as sections of the bottommost material layer. Fig. 6 shows a bottommost material layer having a reference character 11.) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on a bottom surface of the sheet and a plurality of conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and lower conducing traces 11 (see Fig. 11);

a plurality of non-plated vent holes 7 (col. 6, ln 4-7 - "vapor holes 7") through the sheet (see Fig. 11);

a layer of solder resist 5 (col. 5, ln 53-55) covering the lower surfaces of the sheet (see Fig. 11), but leaving the contact areas 10 free from solder resist 5; and

a semiconductor chip 2 including an active surface (Fig. 11 shows a surface facing the sheet 1) with a plurality of chip contact areas (col. 6, ln 33-34 - "electrodes of the semiconductor chip") electrically connected to the sheet 1, wherein non-plated vent holes 7 are disposed in an area A of the sheet directly underneath the semiconductor chip 2 (Annotated Fig. 11 of Takeda shows two vapor holes situated directly underneath the center of the semiconductor chip 2.) and in areas B, B' of the sheet 1 adjacent to but not directly underneath the semiconductor chip 2 (Annotated Fig. 11 of Takeda shows a vapor hole 7 formed in an area Bto the left of the mounting area and another vapor hole 7 formed in an area B' to the right of the mounting area.).

Takeda does not disclose a layer of solder resist covering the upper surface of the substrate.

However, Takamichi teaches a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C) covering an upper surface of a substrate 21 (col. 4, ln 8-10).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate of Takeda with the layer of solder resist covering the upper surface of the substrate as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

As a consequence of the modification, the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the vent holes at the upper surface.

Regarding claim 31, Takeda further teaches the chip 2 that is encapsulated by mold material 3 (col. 6, ln 36-41; see Fig. 11).

Regarding claim 32, Takeda further teaches the chip 2 that is mounted to the sheet 1 by flip-chip technique (see Fig. 11).

Regarding claim 33, Takeda teaches a substrate 1 (col. 6, ln 26-36) for a semiconductor package (see Fig. 11) comprising:

a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material") with an upper surface and a bottom surface, the bottom surface covered with a layer of solder resist 5 (col. 5, ln 1-4 - "a solder resist 5"; see Fig. 11);

a plurality of upper conducting traces (Fig. 11 shows the "upper conducting traces" as sections of a third wiring material layer (middle layer) of five wiring material layers. "At Fig. 11, the wiring substrate is like the same as the first example of the embodiment of the present invention, the wiring substrate 1 is a multi-layer wiring substrate..." (col. 6, ln 24-36")); and upper contact pads 12 (col. 6, ln 24-36) on the upper surface (Fig. 11 shows a surface of the third wiring material layer (middle layer).),

a plurality of bottom conductive traces (Fig. 11 shows "lower conductive traces" as section of the bottommost wiring material layer. Fig. 6 shows a bottommost wiring layer having a reference character 11.) and external contact areas 10 (col. 4, ln 55-65 - "a ball electrode terminal 10") on the bottom surface;

a plurality of conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and bottom conducing traces 11 (see Fig. 11);

a plurality of non-plated vent holes 7 (col. 6, ln 4-7 - "vapor holes 7") through the sheet within a chip mounting area A defined on the upper surface (Annotated Fig. 11 of Takeda shows two vapor holes situated directly underneath the chip 2.) and in areas B, B' adjacent to but outside of the chip mounting area A (Annotated Fig. 11 of Takeda shows a vapor hole formed in an area to the left of the mounting area and another vapor hole formed in an area to the right of the mounting area.); and

a layer of solder resist 5 (col. 5, ln 53-55) covering the bottom surfaces of the substrate (see Fig. 11), but leaving the contact areas 10 free from solder resist 5.

Takeda does not disclose a layer of solder resist covering the upper surface of the substrate.

However, Takamichi teaches a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C) covering an upper surface of a substrate 21 (col. 4, ln 8-10).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate of Takeda with the layer of solder resist covering the upper surface of the substrate as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

The modified substrate as taught by the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the vent holes at the upper surface.

Regarding claim 34, Takeda further teaches the vent holes 7 that include solder resist (col. 6, ln 4-11 - "The inside of this vapor hole is filled with epoxy resin or the same material of solder resist...").

Regarding claim 36, Takeda further teaches the plurality of vent holes that are laterally located towards the center of the substrate (Fig. 11 shows two vapor holes situated directly underneath the center of the semiconductor chip 2.).

9. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda and Takamichi, and further in view of Pub. No. US 2001/0042908 A1 to Okada et al. (hereinafter "Okada").

Regarding claim 20, neither Takeda nor Takamichi discloses the vent holes that are formed by drilling.

However, Okada teaches forming vent holes 16 by drilling (para [0052]).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide for vent holes of Takeda by drilling as taught by Okada as a matter of design choice in light of Okada's teaching that vent holes can be formed by punching (para [0052]), lasing (para [0064]) and drilling (para [0052]).

Regarding claim 21, neither Takeda nor Takamichi discloses forming the vent holes in the core material before forming a plurality of upper contact traces and upper contact pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and depositing conducting vias.

However, Okada teaches forming vent holes 16 in the core material 6 before a plurality of upper contact traces and upper contact pads on its surface, a second

plurality of lower conducting traces and external contact areas on its bottom surface and depositing conducting vias (para [0052] - "...the semiconductor device shown in Fig. 5 has a plurality of vent holes (through holes) 16 previously formed in an organic substrate 6...").

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Takeda with forming the vent holes in the core material before forming contact traces, contact pads, external contact areas and conducting vias as taught by Okada, in order to simply the method of assembling a semiconductor package by not having to form the vent holes after forming contact and conducting features.

10. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda and Takamichi, and further in view of Pub. No. 2002/0043721 A1 to Weber et al. (hereinafter "Weber").

Regarding claim 22, Takeda teaches a method comprising:

providing a substrate 1 comprising a sheet of core material (col. 4, ln 66 - col. 5, ln 4 - "polyimide film or a glass epoxy type resin material") and a plurality of upper contact traces (Fig. 11 shows the "upper conducting traces" as sections of a third wiring material layer (middle layer) of the five wiring material layers. "At Fig. 11, the wiring substrate is like the same as the first example of the embodiment of the present invention, the wiring substrate 1 is a multi-layer wiring substrate..." (col. 6, ln 24-36")) and upper contact pads 12 (col. 6, ln 24-26) on its upper surface (see Fig. 11), a second plurality of lower conducting traces 11 (Fig. 11 shows "lower conductive traces" as

sections of the bottommost wiring material layer. Fig. 6 shows a bottommost material layer having a reference character 11.) and external contact areas 10 (col. 4, ln 55-65 - "ball electrode terminal 10") on its bottom surface and conducting vias 9 (col. 5, ln 19-24) connecting the upper conducting traces and lower conducting traces 11 (see Fig. 11);

forming a plurality of non-plated vent holes 7 (col. 6, ln 4-7 - "vapor holes 7") in the substrate 1;

covering the lower surface of the substrate 1 with a layer of solder resist 5 (col. 5, ln 53-55), but leaving the contact areas 10 free from solder resist 5 (see Fig. 11);

providing a semiconductor chip 2 comprising an active surface (Fig. 11 shows a surface facing the sheet 1) including a plurality of chip contact areas (col. 6, ln 33-34 - "electrodes of the semiconductor chip");

mounting the chip 2 on the upper surface of the substrate 1 by microscopic solder balls 12 (col. 6, ln 32-33 - "a bump 12 using solder") between the chip contacts and upper contact areas, wherein non-plated vent holes 7 are disposed in an area of the substrate directly underneath the semiconductor chip 2 (Annotated Fig. 11 of Takeda shows two vapor holes 7, 7 situated directly underneath the center of the semiconductor chip 2.) and in area B, B' adjacent but not directly underneath the semiconductor chip 2 (Annotated Fig. 11 of Takeda shows a vapor hole 7 formed in an area B to the left of the mounting area A and another vapor hole 7 formed in an area B' to the right of the mounting area A.); and

underfilling the area between the chip 2 and the upper surface of the substrate 1 with epoxy resin 3 (col. 6, ln 36-41; see Fig. 11).

Takeda does not disclose a method of covering the upper surface of the substrate with a layer of solder resist.

However, Takamichi teaches a method of covering an upper surface of a substrate 21 (col. 4, ln 8-10) with a layer of solder resist 25 (col. 4, ln 15-18; see Figs. 1 and 3C).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Takeda with the method of covering the upper surface of the substrate with the layer of solder resist as taught by Takamichi, in order to prevent "an adhesive agent from flowing into the vent hole in the die-bonding process, so that gas permeability can be ensured in the vent hole." (Takamichi, col. 3, ln 9-11).

As a consequence of the modification, the combination of Takeda and Takamichi teaches the layer of solder resist covering the upper surface that closes an end of the vent holes at the upper surface.

Neither Takeda nor Takamichi discloses performing a solder reflow.

However, Weber teaches performing a solder reflow (para [0008]).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method as taught by the combination of Takeda and Takamichi with performing a solder reflow as taught by Weber, so as to electrically contact the semiconductor chip with circuit traces of the substrate (Weber, para [0008]).

Regarding claim 23, Takeda further teaches covering the upper surface of the chip 2 and the substrate1 with a mold material 3 (col. 6, ln 36-41; see Fig. 11).

Conclusion

The previous 35 U.S.C. 103(a) rejections of claims 17, 19-23, 30-34 and 36 have been maintained despite amendments to the claims. Applicant's amendment necessitated the new ground(s) of rejection of claims 24, 25 and 27-29 presented in this Office action.

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL JUNG whose telephone number is (571) 270-3345. The examiner can normally be reached on M-F from 8:00 AM to 7:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL JUNG/
Examiner, Art Unit 2895
19 July 2010

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2895